We claim:

1. A diagnostic read circuit that presents random access memory data of an integrated circuit for external analysis the diagnostic read circuit comprising:

an address generator that addresses and fetches the data stored in the random access memory; and

a data register that temporarily stores the fetched data and that enables transfer of the data fetched from the random access memory for analysis external to the integrated circuit responsive to a control signal.

2. The circuit of claim 1 wherein the data register is coupled to at least one external pin of the integrated circuit.

3. The circuit of claim 2 further including a scan chain coupling the data register to the at least one external pin.

4. The circuit of claim 1 further including a sequence controller that receives the control signal and that causes the address generator to address the random access memory and the data register to store the random access memory data.

5. The circuit of claim 4 wherein the address generator provides random access memory addresses from the integrated circuit for the external analysis.

6. The circuit of claim 5 further including a scan chain coupled to an integrated circuit external pin and wherein the fetched data and the random access memory addresses are transferred through the scan chain to the external pin.

7. The circuit of claim 1 wherein the address generator and data register are within a built-in self-test circuit.

8. A diagnostic read circuit that presents random access memory data of an integrated circuit for analysis external to the integrated circuit, comprising:

an address generator that generates memory addresses of random access memory to obtain the data stored in the random access memory;

a data register for temporarily storing the obtained data;

a sequence controller that controls the address generator and the data register; and at least one external pin carried by the integrated circuit and coupled to the data register that receives the obtained data from the data register.

9. The circuit of claim 8 further including a scan chain coupling the data register to the external pin.

10. The circuit of claim 8 wherein the address generator also provides the memory addresses to the at least one external pin.

11. The circuit of claim 10 further including a scan chain coupled to the at least one external pin and wherein the stored data and the memory addresses are transferred through the scan chain to the at least one external pin.

12. The circuit of claim 13 wherein the address generator and the data register are within a built-in self-test circuit.

13. An integrated circuit comprising:

a random access memory;

an external pin; and

a data register that temporarily stores memory contents of the random access memory and that enables transfer of the memory contents to the external pin.

14. The integrated circuit of claim 13 further including a scan chain coupling the data register to the external pin.

15. The integrated circuit of claim 13 further including an address generator that provides data storage addresses to the random access memory for reading of the memory contents.

16. The integrated circuit of claim 15 wherein the address generator provides the data storage addresses to the external pin.

17. The integrated circuit of claim 16 further including a scan chain coupled to the integrated circuit external pin and wherein the stored memory contents and the data storage addresses are transferred through the scan chain to the external pin.

18. The integrated circuit of claim 15 wherein the address generator and the data register form part of a built-in self-test circuit.

19. In an integrated circuit, a method comprising:
detecting a memory storage error in a random access memory;
reading data stored in the random access memory;
temporarily storing the read data; and
transferring the temporarily stored read data to an external pin of the integrated circuit responsive to detecting a storage error.

20. The method of claim 19 wherein the reading step includes generating memory addresses.

21. The method of claim 20 including the further step of transferring the memory addresses to the external pin.